19-0451; Rev 1; 10/98

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

General Description

The MAX349/MAX350 are 8-channel and dual 4-channel serially controlled multiplexers (muxes). These muxes conduct equally well in either direction. On-resistance (100Ω max) is matched between switches to 16Ω max and is flat (10Ω max) over the specified signal range.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each mux can handle rail-to-rail analog signals. The off-leakage current is only 0.1nA at +25°C or 5nA at +85°C.

Upon power-up, all switches are off and the internal shift registers are reset to zero.

The serial interface is compatible with SPI™/QSPI™ and MICROWIRE™. Functioning as a shift register, it allows data (at DIN) to be clocked in synchronously with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several MAX349s or MAX350s to be daisy chained.

All digital inputs have 0.8V or 2.4V logic thresholds, ensuring both TTL and CMOS-logic compatibility when using ±5V supplies or a single +5V supply.

Applications

Serial Data-Acquisition Systems	Industrial and Process-Control Systems
Avionics	ATE Equipment
Audio Signal Routing	Networking

Features

- **SPI/QSPI, MICROWIRE-Compatible Serial Interface**
- **8 Separately Controlled SPST Switches**
- **Single 8-to-1 Mux (MAX349)**
  Dual 4-to-1 Mux (MAX350)
- **100Ω Signal Paths with ±5V Supplies**
- **Rail-to-Rail® Signal Handling**
- **Asynchronous $\overline{\text{RESET}}$ Input**
- **±2.7V to ±8V Dual Supplies**
  +2.7V to +16V Single Supply
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs (with +5V or ±5V Supplies)**

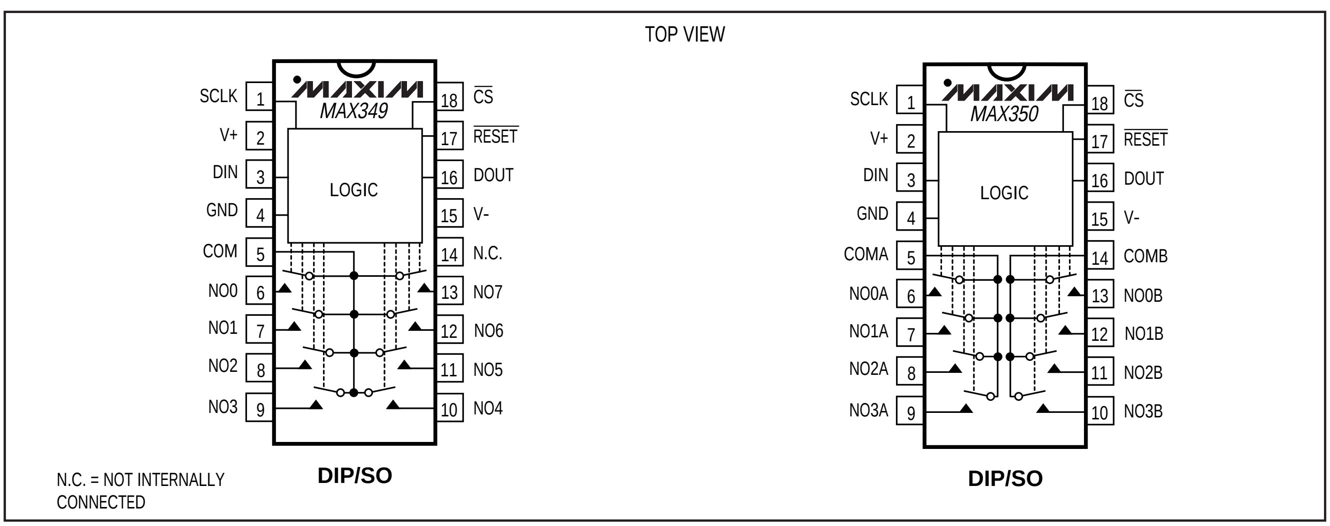
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX349CPN	0°C to +70°C	18 Plastic DIP
MAX349CWN	0°C to +70°C	18 Wide SO
MAX349CAP	0°C to +70°C	20 SSOP
MAX349C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams



Pin Configurations continued at end of data sheet.

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
- V+ ....-0.3V, +17V
- V- ....-17V, +0.3V
- V+ to V-....................-0.3V, +17V
- SCLK, $\overline{CS}$, DIN, DOUT, $\overline{RESET}$ ....-0.3V to (V+ + 0.3V)
- NO, COM ....(V- - 2V) to (V+ + 2V)

Continuous Current into Any Terminal....................±30mA
Peak Current, NO or COM
- (pulsed at 1ms, 10% duty cycle)....................±100mA

Continuous Power Dissipation (T_A = +70°C)
- 18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) ..889mW
- 18-Pin SO (derate 9.52mW/°C above +70°C)..............762mW
- 20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
- 18-Pin CERDIP (derate 10.53mW/°C above +70°C).....842mW

Operating Temperature Ranges
- MAX349C_ _, MAX350C_ _ ....0°C to +70°C
- MAX349E_ _, MAX350E_ _....................-40°C to +85°C
- MAX349M_ _, MAX350M_ _ ....-55°C to +125°C

Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM-NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA		T_A = +25°C		60	100	Ω
				C, E, M			125	
COM-NO On-Resistance Match Between Channels (Note 2)	ΔR_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA		T_A = +25°C			16	Ω
				C, E, M			20	
COM-NO On-Resistance Flatness (Note 2)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V		T_A = +25°C			10	Ω
				C, E, M			15	
NO Off-Leakage Current (Note 3)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V		T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-10		10	
		V+ = 5.5V, V- = -5.5V, V_{COM} = 4.5V, V_{NO} = -4.5V		T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-10		10	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} = ±4.5V	MAX349	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V	MAX349	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-5		5	
				M	-50		50	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM} = V_{NO}$ = ±4.5V	MAX349	T_A = +25°C	-0.2	0.001	0.2	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.02	0.2	
				C, E	-5		5	
				M	-50		50	
DIGITAL I/O								
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}			C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}			C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA		C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$			C, E, M		100		mV
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$		T_A = +25°C		200	275	ns
				C, E, M			400	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$		T_A = +25°C		90	150	ns
				C, E, M			300	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$		T_A = +25°C	5	40		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω		T_A = +25°C		1	10	pC
NO Off-Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz		T_A = +25°C		2		pF
COM Off-Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz		T_A = +25°C		2		pF
Switch On-Capacitance	$C_{(ON)}$	$V_{COM} = V_{NO}$ = GND, f = 1MHz		T_A = +25°C		8		pF
Off-Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = 1V_{RMS}, f = 100kHz		T_A = +25°C		> 90		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = 1V_{RMS}, f = 100kHz		T_A = +25°C		< -90		dB
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E, M	±3		±8	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+		T_A = +25°C		7	20	µA
				C, E, M			30	
V- Supply Current	I-	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+		T_A = +25°C	-1	0.1	1	µA
				C, E, M	-2		2	

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

TIMING CHARACTERISTICS—Dual Supplies (Figure 1)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time	t_{CSH2}		C, E, M	240			ns
SCLK High Time	t_{CH}		C, E, M	190			ns
SCLK Low Time	t_{CL}		C, E, M	190			ns
Minimum Data Setup Time	t_{DS}		C, E, M		17	100	ns
Data Hold Time	t_{DH}		C, E, M	0	-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off-isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM-NO On-Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{NO} = 1mA		T_A = +25°C		125	175	Ω
				C, E, M			225	
NO Off-Leakage Current (Notes 4, 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V		T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-10		10	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V		T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-10		10	
COM Off-Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V	MAX349	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	MAX349	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-5		5	
				M	-50		50	
COM On-Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = ±4.5V	MAX349	T_A = +25°C	-0.2	0.01	0.2	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.02	0.2	
				C, E	-5		5	
				M	-50		50	
DIGITAL I/O								
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}			C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}			C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA		C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$			C, E, M		100		mV
POWER SUPPLY								
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+		T_A = +25°C		7	20	µA
				C, E, M			30	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

($V+ = +4.5V$ to $+5.5V$, $V- = 0V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at $T_A = +25°C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	$T_A = +25°C$		160	400	ns
			C, E, M			500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	$T_A = +25°C$		60	200	ns
			C, E, M			300	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	$T_A = +25°C$		15		ns
Charge Injection (Note 4)	V_{CTE}	$C_L = 1nF$, $V_{NO} = 0V$, $R_S = 0\Omega$	$T_A = +25°C$		1	10	pC
Off-Isolation (Note 6)	V_{ISO}	$R_L = 50\Omega$, $C_L = 15pF$, $V_{NO} = 1V_{RMS}$, f = 100kHz	$T_A = +25°C$		> 90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	$R_L = 50\Omega$, $C_L = 15pF$, $V_{NO} = 1V_{RMS}$, f = 100kHz	$T_A = +25°C$		< -90		dB

TIMING CHARACTERISTICS—Single +5V Supply (Figure 1)

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Minimum Data Setup Time (Note 4)	t_{DS}		C, E, M		17	100	ns
Data Hold Time (Note 4)	t_{DH}		C, E, M		-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.
Note 4: Guaranteed by design.
Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.
Note 6: See Figure 6. Off-isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.
Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM-NO On-Resistance	R_{ON}	V+ = 3.0V, V_{COM} = 1.5V, I_{NO} = 1mA		T_A = +25°C		270	500	Ω
				C, E, M			600	
COM Off-Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	MAX349	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-50		50	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	MAX349	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.002	0.2	
				C, E	-5		5	
				M	-50		50	
COM On-Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 3.6V, $V_{COM} = V_{NO}$ = 3V	MAX349	T_A = +25°C	-0.2	0.01	0.2	nA
				C, E	-10		10	
				M	-100		100	
			MAX350	T_A = +25°C	-0.2	0.02	0.2	
				C, E	-5		5	
				M	-50		50	
DIGITAL I/O								
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}			C, E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}			C, E			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		C, E	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.1mA		C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA		C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$			C, E, M		100		mV
POWER SUPPLY								
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or 5V		T_A = +25°C		6	20	µA
				C, E, M			30	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 4)	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		275	600	ns
			C, E, M			700	
Turn-Off Time (Note 4)	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		120	300	ns
			C, E, M			400	
Break-Before-Make Delay (Note 4)	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C	5	15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		1	10	pC
Off-Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{NO} = 1V_{RMS}$, f = 100kHz	T_A = +25°C		> 90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{NO} = 1V_{RMS}$, f = 100kHz	T_A = +25°C		< –90		dB

TIMING CHARACTERISTICS—Single +3V Supply (Figure 1)

($V+ = +3.0V$ to $+3.6V$, $V- = 0V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at $T_A = +25°C$.)

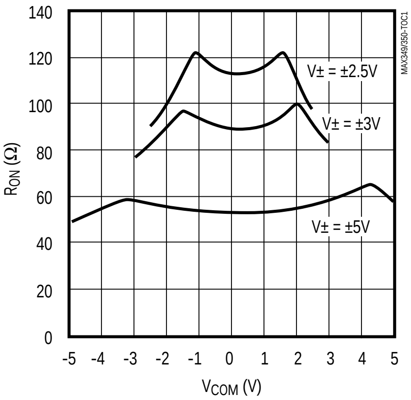
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Minimum Data Setup Time (Note 4)	t_{DS}		C, E, M		38	120	ns
Data Hold Time (Note 4)	t_{DH}		C, E, M		-38		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, $C_L = 10pF$	$T_A = +25°C$		150		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, $C_L = 10pF$	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, $C_L = 10pF$	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, $C_L = 10pF$	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, $C_L = 10pF$	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width (Note 4)	t_{RW}		$T_A = +25°C$		105		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.
Note 4: Guaranteed by design.
Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.
Note 6: See Figure 6. Off-isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.
Note 7: Between any two switches. See Figure 3.

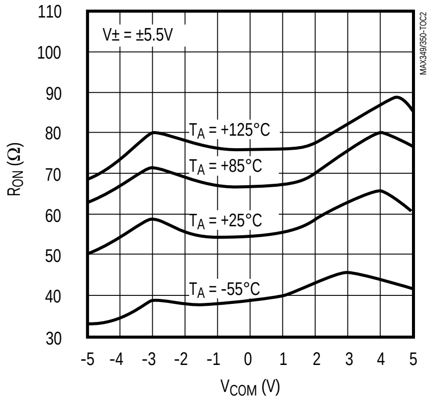
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

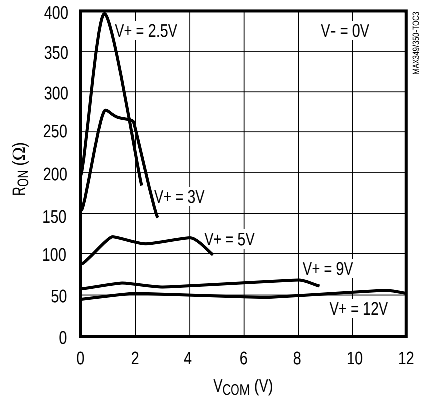
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



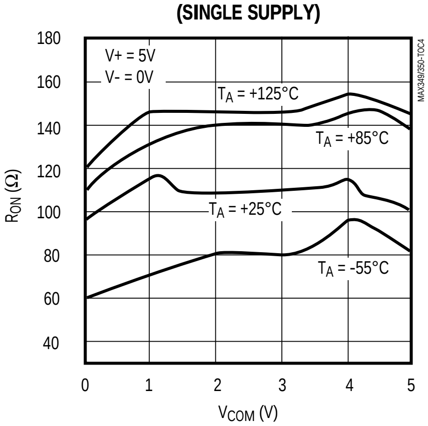
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



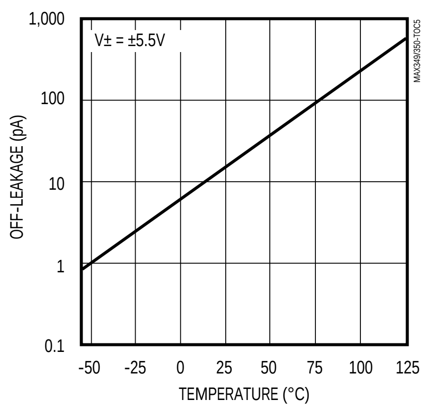
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



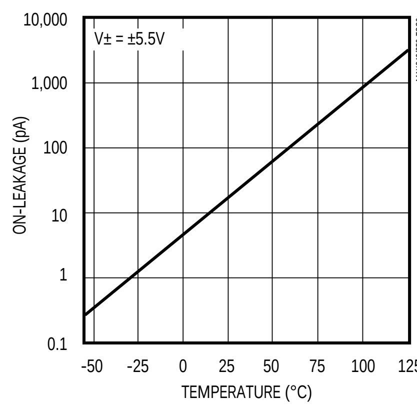
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



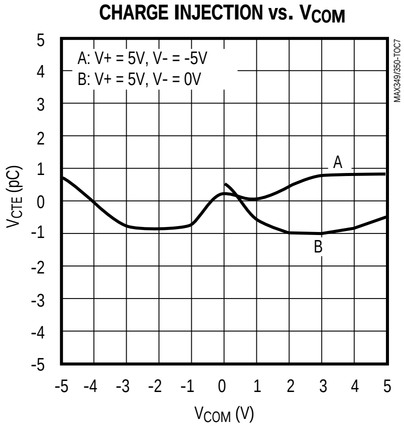
OFF-LEAKAGE vs. TEMPERATURE



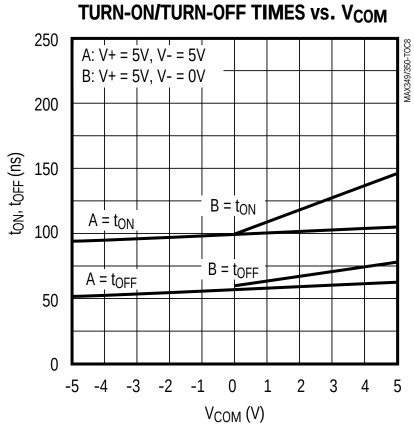
ON-LEAKAGE vs. TEMPERATURE



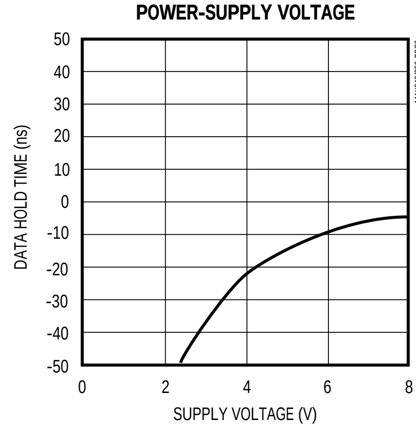
CHARGE INJECTION vs. V_{COM}



TURN-ON/TURN-OFF TIMES vs. V_{COM}



DATA HOLD TIME vs. POWER-SUPPLY VOLTAGE

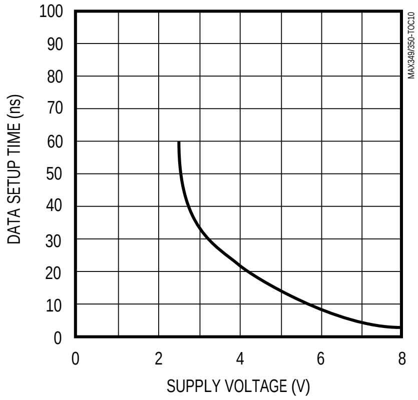


Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

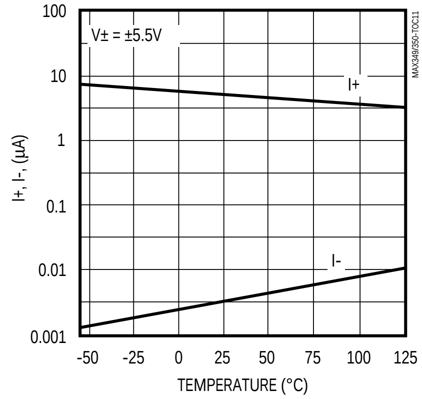
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

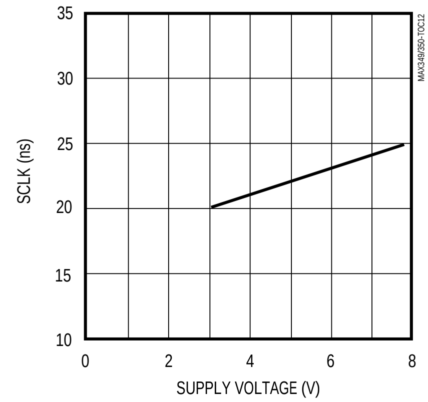
DATA SETUP TIME vs. POSITIVE SUPPLY VOLTAGE



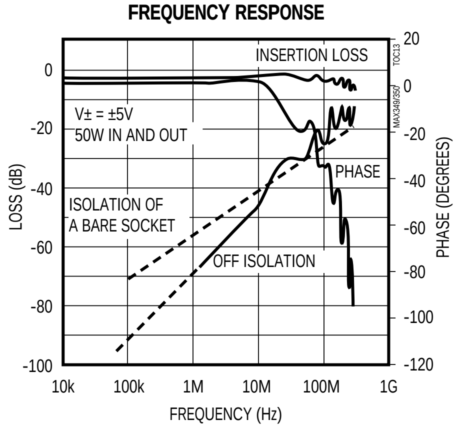
POWER-SUPPLY CURRENT vs. TEMPERATURE



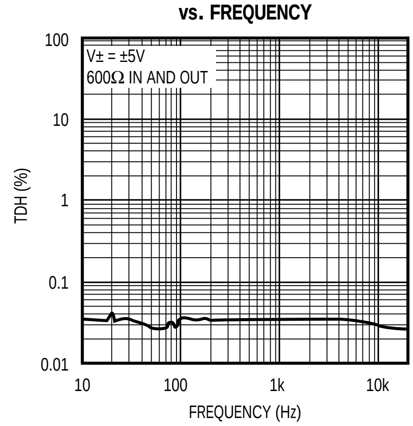
MINIMUM SCLK PULSE WIDTH vs. POSITIVE SUPPLY VOLTAGE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN				NAME	FUNCTION
MAX349		MAX350			
DIP/SO	SSOP	DIP/SO	SSOP		
1	1	1	1	SCLK	Serial Clock Digital Input
2	2	2	2	V+	Positive Analog Supply Voltage Input
3	3	3	3	DIN	Serial Data Digital Input
4	4	4	4	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
5	5	—	—	COM	Common Analog Switch (mux output)
6–13	6–9, 11–14	—	—	NO0–NO7	Normally Open Analog Switch Inputs 0–7
—	—	5	5	COMA	Common Analog Switch “A” (mux output)
—	—	6–9	6–9	NO0A–NO3A	Normally Open Analog Switch “A” Inputs 0–3
—	—	10–13	11–14	NO3B–NO0B	Normally Open Analog Switch “B” Inputs 0–3
—	—	14	15	COMB	Common Analog Switch “B” (mux output)
14	10, 15, 16	—	10, 16	N.C.	No Connect, not internally connected.
15	17	15	17	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
16	18	16	18	DOUT	Serial Data Digital Output. Output high is V+.
17	19	17	19	$\overline{\text{RESET}}$	RESET Input. Connect to logic high (or V+) for normal operation. Drive low to set all switches off and set internal shift registers to 0.
18	20	18	20	$\overline{\text{CS}}$	Chip-Select Digital Input (Figure 1)

Note: *NO and COM pins are identical and interchangeable. Either may be considered as an input or an output; signals pass equally well in either direction.*

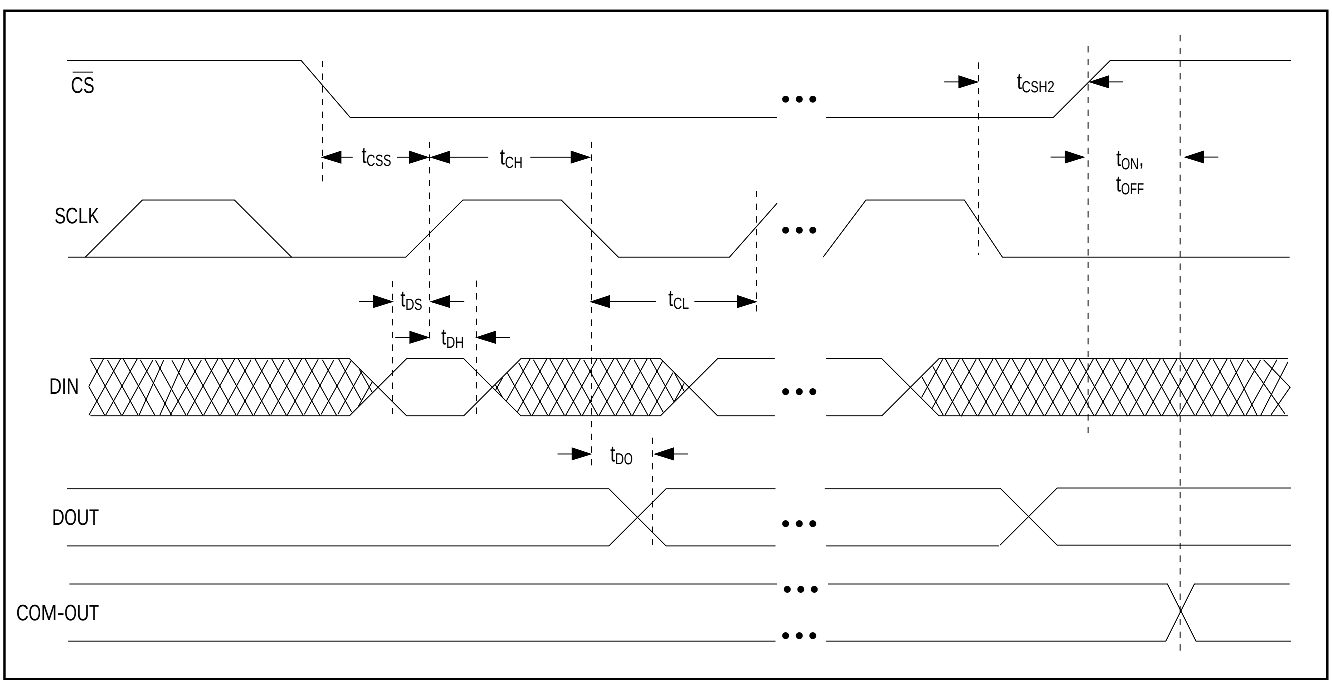


Figure 1. Timing Diagram

Serially Controlled, Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers

Detailed Description

Basic Operation

The MAX349/MAX350 are 8-channel and dual 4-channel, serially controlled multiplexers (muxes). These muxes are unusual in that any, all, or none of the input channels can be directed to the output. All switches are bidirectional, so inputs and outputs are interchangeable. When multiple inputs are connected to an output, they are also connected to one another, separated from each other only by the on-resistance of two switches. Both parts require eight bits of serial data to set all eight switches.

Serial Digital Interface

The MAX349/MAX350 interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$ (Figure 2). While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronously with SCLK's rising edge. The input is an 8-bit word, each bit controlling one of the eight switches (Tables 1 and 2). DOUT is the output of the shift register, with data appearing synchronously with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their previous configuration. When the eight bits of data have been shifted in, $\overline{CS}$ is driven high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when CS is high, and DOUT holds the first input bit (D7) at its output.

More or fewer than eight clock cycles can be entered during the $\overline{CS}$ low period. When this happens, the shift register contains only the last eight serial data bits, regardless of when they were entered. On the rising edge of $\overline{CS}$, all switches are set to the corresponding states.

The MAX349/MAX350 three-wire serial interface is compatible with SPI, QSPI, and MICROWIRE standards. If interfacing with a Motorola processor serial interface, set CPOL = 0. The MAX349/MAX350 are considered to be slave devices (Figures 2 and 3). At power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state. This meets all SPI and QSPI requirements.

Daisy-Chaining

For a simple interface using several MAX349s and MAX350s, "daisy-chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected, and a stream of data is shifted through the MAX349s or MAX350s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the MAX349/MAX350 data chain. Note that the DOUT high level is V+, which may not be compatible with TTL/CMOS devices if V+ differs from the logic supply for these other devices.

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each decode logic individually control $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ pin is driven low, data is shifted in, and $\overline{CS}$ is driven high to latch the data. Typically, only one slave is addressed at a time. DOUT is not used.

Applications Information

8x1 Multiplexer

The MAX349 can be programmed normally, with only one channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, select the channels by sending a single high pulse (corresponding to the selected channel) at DIN, and a corresponding $\overline{CS}$ low pulse for every eight clock pulses. As SCLK clocks this through the register, each switch sequences one channel at a time, starting with channel 0.

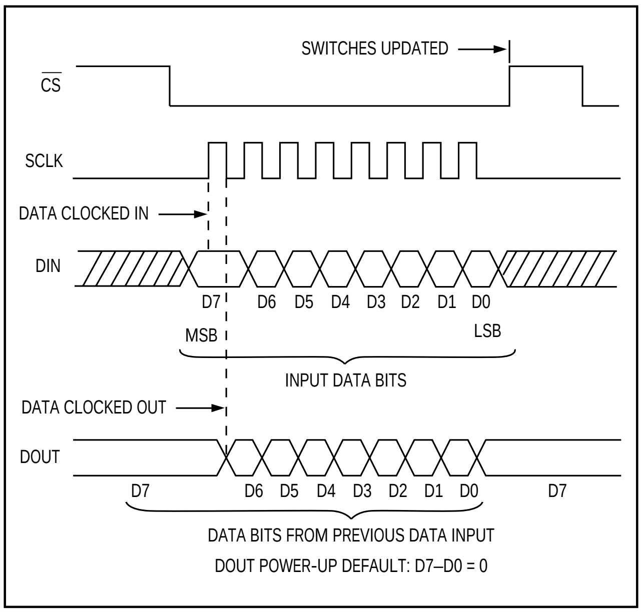


Figure 2. 3-Wire Interface Timing

Table 1. MAX349 Serial-Interface Switch Programming

RESET	DATA BITS								MAX349 FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	0	0	0	0	0	0	0	All switches open, D7–D0 = 0
1	1	1	1	1	1	1	1	1	All switches closed to COM, D7–D0 = 1
1	**0**	X	X	X	X	X	X	X	Switch 7 open (off)
1	**1**	X	X	X	X	X	X	X	Switch 7 closed to COM
1	X	**0**	X	X	X	X	X	X	Switch 6 open (off)
1	X	**1**	X	X	X	X	X	X	Switch 6 closed to COM
1	X	X	**0**	X	X	X	X	X	Switch 5 open (off)
1	X	X	**1**	X	X	X	X	X	Switch 5 closed to COM
1	X	X	X	**0**	X	X	X	X	Switch 4 open (off)
1	X	X	X	**1**	X	X	X	X	Switch 4 closed to COM
1	X	X	X	X	**0**	X	X	X	Switch 3 open (off)
1	X	X	X	X	**1**	X	X	X	Switch 3 closed to COM
1	X	X	X	X	X	**0**	X	X	Switch 2 open (off)
1	X	X	X	X	X	**1**	X	X	Switch 2 closed to COM
1	X	X	X	X	X	X	**0**	X	Switch 1 open (off)
1	X	X	X	X	X	X	**1**	X	Switch 1 closed to COM
1	X	X	X	X	X	X	X	**0**	Switch 0 open (off)
1	X	X	X	X	X	X	X	**1**	Switch 0 closed to COM

Table 2. MAX350 Serial-Interface Switch Programming

RESET	DATA BITS								MAX350 FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	0	0	0	0	0	0	0	All switches open, D7–D0 = 0
1	1	1	1	1	1	1	1	1	All “A” switches closed to COMA; All “B” switches closed to COMB, D7–D0 = 1
1	**0**	X	X	X	X	X	X	X	Switch NO0B open (off)
1	**1**	X	X	X	X	X	X	X	Switch NO0B closed
1	X	**0**	X	X	X	X	X	X	Switch NO1B open (off)
1	X	**1**	X	X	X	X	X	X	Switch NO1B closed
1	X	X	**0**	X	X	X	X	X	Switch NO2B open (off)
1	X	X	**1**	X	X	X	X	X	Switch NO2B closed
1	X	X	X	**0**	X	X	X	X	Switch NO3B open (off)
1	X	X	X	**1**	X	X	X	X	Switch NO3B closed
1	X	X	X	X	**0**	X	X	X	Switch NO3A open (off)
1	X	X	X	X	**1**	X	X	X	Switch NO3A closed
1	X	X	X	X	X	**0**	X	X	Switch NO2A open (off)
1	X	X	X	X	X	**1**	X	X	Switch NO2A closed
1	X	X	X	X	X	X	**0**	X	Switch NO1A open (off)
1	X	X	X	X	X	X	**1**	X	Switch NO1A closed
1	X	X	X	X	X	X	X	**0**	Switch NO0A open (off)
1	X	X	X	X	X	X	X	**1**	Switch NO0A closed

X = Don’t care. Data bit D7 is first bit in; data bit D0 is last in.

Dual, Differential 4-Channel Multiplexer

The MAX350 can be programmed normally, with only one differential channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, select the channels by sending two high pulses, spaced four clock pulses apart (corresponding to the two selected channels) at DIN, and a corresponding $\overline{CS}$ low pulse for each of the first eight clock pulses. As SCLK clocks this through the register, each switch sequences one differential channel at a time, starting with channel 0. Repeat this process for subsequent channel sequencing after the first eight bits have been sent. For even faster channel sequencing, send only one DIN high pulse and one $\overline{CS}$ low pulse for every four clock pulses.

Reset Function

$\overline{RESET}$ is the internal reset pin. It is usually connected to a logic signal or V+. Drive $\overline{RESET}$ low to open all switches and set the contents of the internal shift register to zero simultaneously. When $\overline{RESET}$ is high, the part functions normally and DOUT is sourced from V+. $\overline{RESET}$ must not be driven beyond V+ or GND.

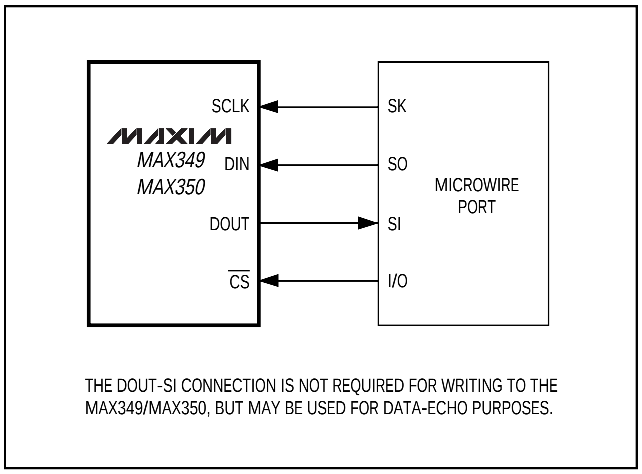


Figure 3. Connections for MICROWIRE

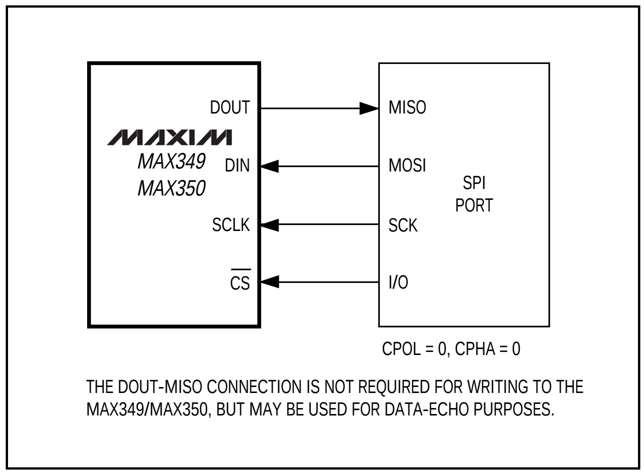


Figure 4. Connections for SPI and QSPI

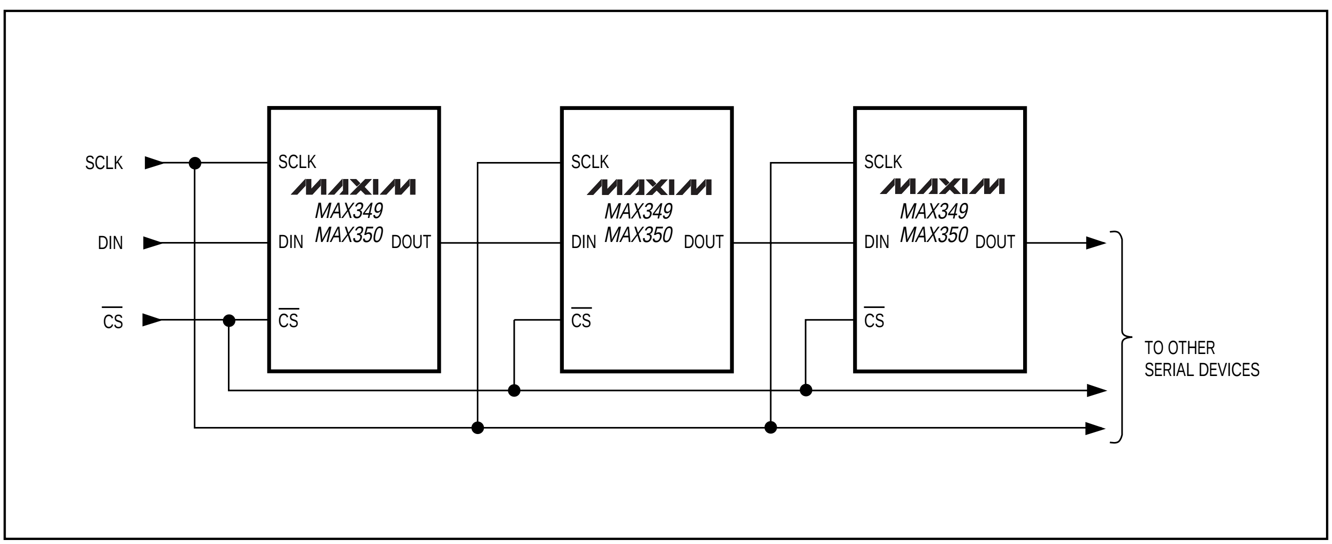


Figure 5. Daisy-Chained Connection

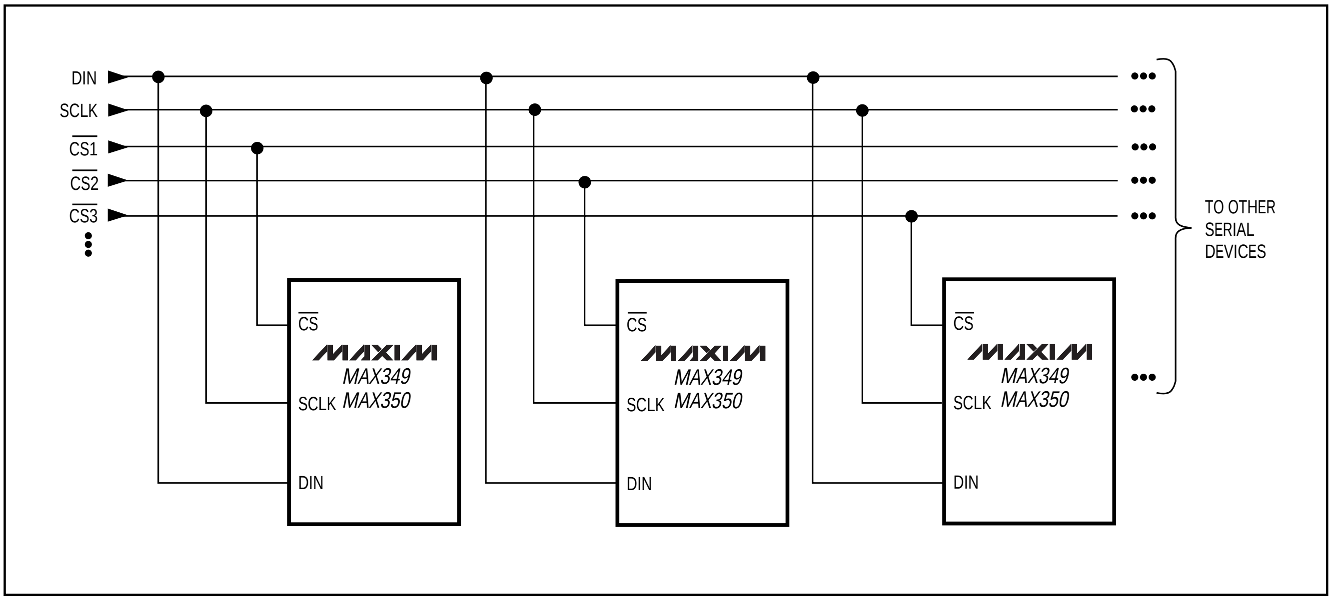


Figure 6. Addressable Serial Interface

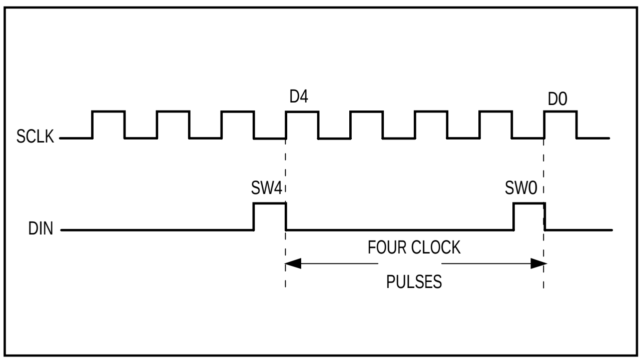


Figure 7. Differential Multiplexer Input Control

Power-Supply Considerations

Overview

The MAX349/MAX350 construction is typical of most CMOS analog switches. It has three supply pins: V+, V- and GND. V+ and V- are used to drive the internal CMOS switches, and they set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog signal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ rises, the threshold increases slightly. Therefore, when V+ reaches +12V, the threshold is about 3.1V; above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX349/MAX350 operate with bipolar supplies from ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 17V. **Do not connect the MAX349/MAX350 V+ to +3V and connect the logic-level pins to TTL logic-level signals. This exceeds the absolute maximum ratings and can damage the part and/or external circuits.**

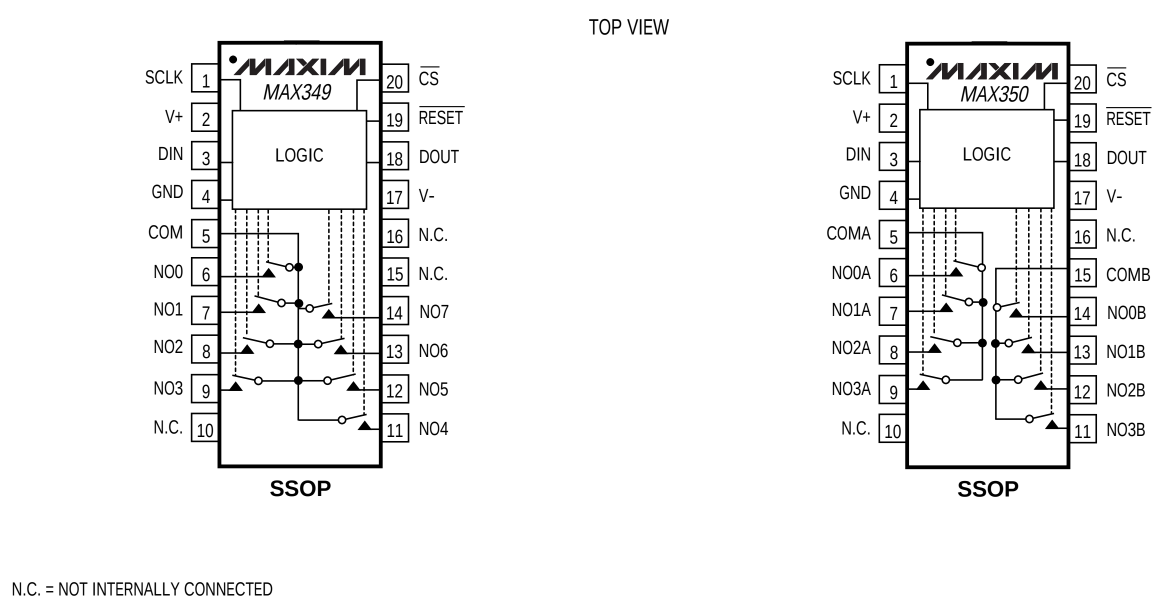
Single Supply

The MAX349/MAX350 operate from single supplies between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics)*. Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off-isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is entirely due to capacitive coupling.

Pin Configurations/Functional Diagrams (continued)



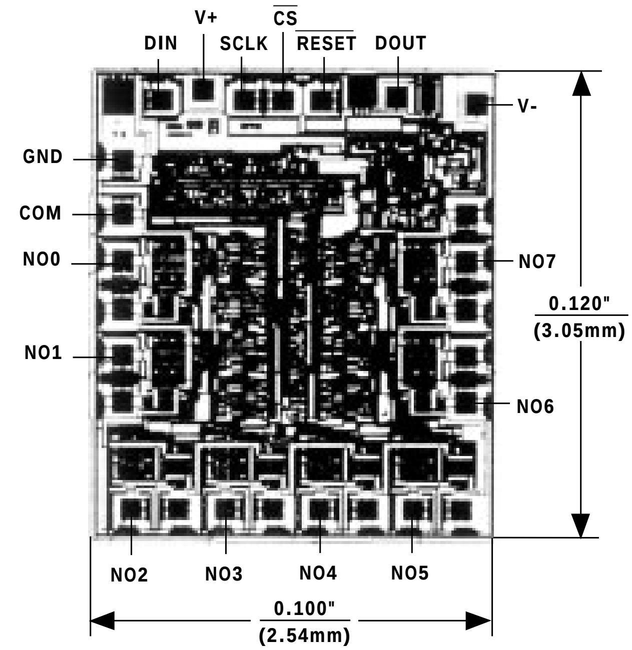
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX349EPN	-40°C to +85°C	18 Plastic DIP
MAX349EWN	-40°C to +85°C	18 Wide SO
MAX349EAP	-40°C to +85°C	20 SSOP
MAX349MJN	-55°C to +125°C	18 CERDIP**
MAX350CPN	0°C to +70°C	18 Plastic DIP
MAX350CWN	0°C to +70°C	18 Wide SO
MAX350CAP	0°C to +70°C	20 SSOP
MAX350C/D	0°C to +70°C	Dice*
MAX350EPN	-40°C to +85°C	18 Plastic DIP
MAX350EWN	-40°C to +85°C	18 Wide SO
MAX350EAP	-40°C to +85°C	20 SSOP
MAX350MJN	-55°C to +125°C	18 CERDIP**

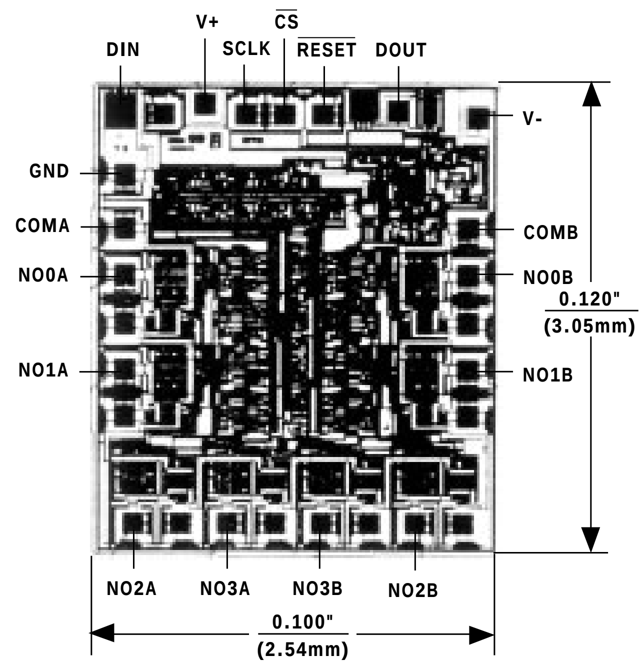
* *Contact factory for dice specifications.*
** *Contact factory for availability.*

Chip Topographies

MAX349

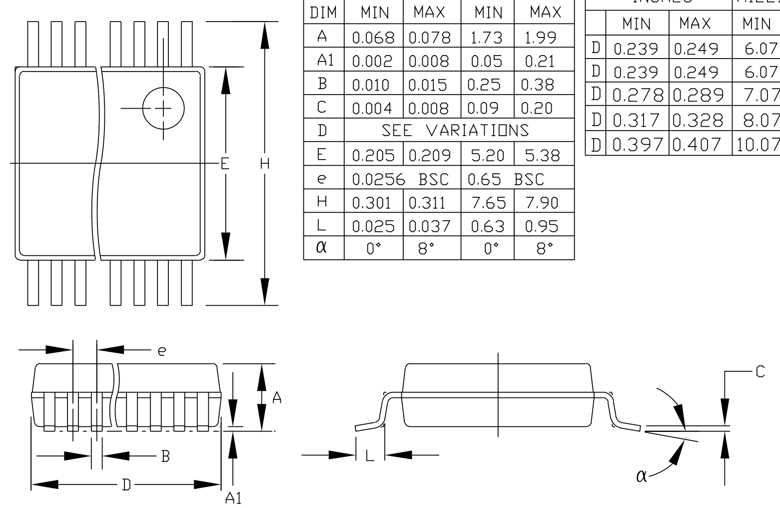


MAX350



TRANSISTOR COUNT: 500
SUBSTRATE CONNECTED TO V+.

Package Information

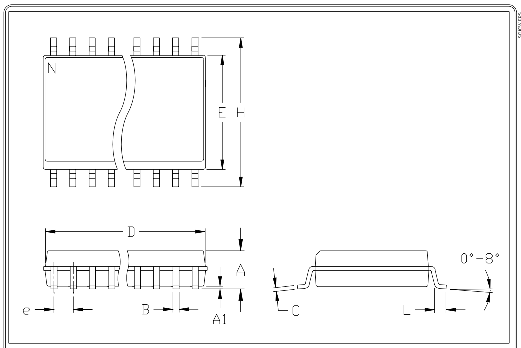


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SSOP, 5.3X.65mm
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV A | 1/1



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION
PACKAGE FAMILY OUTLINE: SOIC .300" | TITLE | 1/1 | 21-0042 A | DOCUMENT CONTROL NUMBER | REV

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